REMARKS

Applicant expresses appreciation to the Examiner for consideration of the subject patent application. This amendment is in response to the Office Action mailed June 13, 2005. Claims 6, 7, and 13 were objected to. Claims 1-5 and 8-12 were rejected.

Claims 1-13 were originally presented. Claims 1-13 remain in the application. No claims have been amended.

The indication of allowable subject matter in claims 6, 7, and 13, if rewritten in independent form, is acknowledged with appreciation.

Claim Rejections - 35 U.S.C. § 103

Claims 1-3, 8, and 10 (including independent claims 1 and 10) were rejected under 35 U.S.C. § 103 as being unpatentable over Williams et al. (US 2004/0207618) (hereinafter "Williams" in view of Simmonds et al. (US 6,646,645) (hereinafter "Simmonds") and further in view of Srivastava (US 5,121,086).

Summary of the Patents

Williams discloses a method of aligning slave modules with an external synchronization signal. Williams verifies that the internal clock matches the external sync signal (Williams 0008, 0088). If the internal clock does not match the external sync signal, the internal clock is reset to match the external sync signal (Williams 0008, 0088). Williams does not verify that the signal is accurate. Williams specifically rejects an Ethernet network as the medium for the sync signal, by verifying that the synchronization input/output ports are not connected to an Ethernet network (Williams 0095). This teaches away for the present application, which is designed to accept delays in the synchronization signal.

Simmonds teaches a method of synchronizing display outputs with an external synchronization signal (Simmonds Abstract). Simmonds receives a reference clock and raster sync input from an external sync card and distributes it internally (Simmonds Abstract). As part of this distribution, Simmonds uses a counter to count either scanline positions or clock cycles since the VSYNC from the graphics processor (Simmonds col. 4, line 37-48). Using registers

and comparators, Simmonds uses the output of the counter to detect before and after a buffer swap is performed by the graphics processor (Simmonds col. 4, lines 40-43). This detection allows the master synchronization card to avoid a race hazard (Simmonds col. 11, lines 4-12). Simmonds does not use the registers to hold an external synchronization signal or an array of timestamps of an external synchronization signal, but stores buffer swap timing as the number of clocks or scanlines since VSYNC from the internal graphics processor (Simmonds col. 4, lines 37-48). Simmonds does not verify the validity of the external synchronization signal, but merely determines if the sync card should send a master synchronization signal or receive a slave synchronization signal (Simmonds col. 4, lines 14-20).

Srivastava discloses a method of removing static error from an oscillator control system (Srivastava col. 3, lines 15-18) by appropriate long term change or shift of the steady state or free running frequency of the oscillator (Srivastava col. 8, lines 61-64) which is applied in a television reciever receive a channel (col. 3, line 40-66). Prior art oscillator control systems would develop static phase error when adjusting to a substantial frequency difference. To remedy this static phase error problem, Srivastava method includes a threshold detector and error integrator. The threshold detector detects large frequency corrections and averages these corrections over a vertical scan interval (Srivastava col. 6, lines 1-4). The error integrator averages over the vertical pulse period the number of horizontal output pulses the up/down counter goes up or down. (Srivastava col. 8, lines 50-53). As a result, the invention produces an appropriate long term change or shift of the steady state or free running frequency of the oscillator (Srivastava col. 8, lines 61-64). Srivastava does not disclose computing average sync signal timing comparisons, but averages the output pulses on an up/down counter through a circuit (Srivastava col. 8, lines 50-53). Srivastava does not decide that the incoming synchronization signal is valid; instead, Srivastava uses the threshold as a method to determine when the invention should produce a long term change in the steady state of the oscillator instead of a short term change (col. 6, lines 60-64, col. 8, lines 61-65).

Applicant discloses a system and method for determining whether an incoming synchronization signal should be used for synchronization (Application Claim 1). Applicant stores the last n previously received synchronization signals in an array where n is the size of the

array (Application Claim 1). Synchronization signals travel across a network (Application page 3, lines 6-7) that may have a transimission delay (Application page 3, lines 22-23). Applicant compares a newly arrived synchronization signal against the array of previously received synchronization signals (Application Claim 1). Applicant then replaces the oldest of the n synchronization signals in the array with the new synchronization signal (Application Claim 1). If the comparisons of the n synchronization signals are on average above a preset threshold, the synchronization signals are considered valid (Application Claim 1).

Combination does not contain all the elements

The combination of Williams, Simmonds and Srivastava do not contain all the elements of Applicant's claims. The Office Action asserts that the combination of Williams, Simmonds and Srivastava teach the elements of (1) receiving a stream of at least n sync signals from the remote computer (Williams), (2) storing the most recently received n sync signals in an array (Simmonds), (3) comparing an n + 1 sync signal with each of the n sync signals in the array to form a comparison for each of the n sync signals in the array (Williams and Simmonds (signals stored in array)), (4) replacing the oldest of the n sync signals in the array with the n + 1 sync signal (Williams) and (5) using the n + 1 sync signal to synchronize the at least one graphics processing card in each graphics processing computer with each at least one graphics processing card in the plurality of graphics processing computers if the comparisons of the n sync signals in the array are greater on the average than a preset threshold (Srivastava). Examination of these elements will show that the cited art do not teach these elements.

(1) Williams does not teach "receiving a stream of at least n sync signals from the remote computer", as recited in claim 1. The Office Action asserts that "The external synchronization signal has a phase [0087], and this phase inherently refers to the spacing of the sync signals in the external synchronization signal. Therefore, Williams describes receiving a stream of at least n sync signals from the remote computer." While Williams does examine phase differences between the internal clock and the external synchronization signal, Williams simply adjusts the internal clock to match the external synchronization signal (Williams ¶ 0088). Williams does not disclose that they require at least n sync signals from the remote computer to match phase. In

contrast, the present application uses n sync signals to account for network or buss delays.

The sync signal medium required by Williams is limiting compared to mediums disclosed in Applicant's application. Williams requires that the sync signal be provided with minimal delay due to the assumption that the sync signal is correct, while Applicant is able to use a network with transmission delay. In fact, Williams specifically rejects an Ethernet network as the medium for the sync signal, by verifying that the synchronization input/output ports are not connected to an Ethernet network (Williams ¶ 0095). In contrast, Applicant's synchronization signals travel across a network (Application page 3, lines 6-7) that may have a transmission delay (Application page 3, lines 22-23). Thus, use of Ethernet is acceptable in the present application.

(2) Simmonds does not disclose "storing the most recently received n sync signals in an array" as claimed. The Office Action asserts that "The selected scanline locations are preferably programmed into the registers (146, 148, Figure 6; Col. 10, lines 26-28) ... Therefore, the values stored in the registers or array are the most recently received n sync signals. The signals are then compared (Col. 10, lines 37-46)."

However, the registers disclosed in Simmonds do not store sync signals, but simply hold values that will aid in avoiding a "Buffer Swap Race Hazard" (Simmonds col. 9, line 55). The registers hold values that will be used in conjunction with comparators and a counter to cause two interrupts (Simmonds col. 10, lines 18-29) which makes sure that the video raster is not between the two specified interrupt positions (Simmonds col. 10, lines 63-67) which can cause a Buffer Swap Race Hazard (Simmonds col. 11, lines 1-12). The register values are also derived from the last vertical sync (VSYNC) from the graphics processor (Simmonds, col. 4, line 39) and not the external synchronization signal. Therefore, the registers do not contain values from the external sync signal, nor do the registers contain an array of n sync signals.

(3) Williams in view of Simmonds does not disclose the claimed operation of "comparing an n + 1 sync signal with each of the n sync signals in the array to form a comparison for each of the n sync signals in the array." Simmonds does not disclose an array of external sync signals. In addition, Williams and Simmonds do not disclose a comparison of n sync signals, and neither Williams nor Simmonds discloses a comparison of an n+1 sync signal with n sync signals. The Office Action asserts "The clock signals of the graphics modules are the n sync

signals since they are inherently the signals that were received previously, and the external synchronization signal is the n + 1 sync signal since it is the signal that is received next. Therefore, Williams describes comparing an n + 1 sync signal with each of the n sync signals to form a comparison for each of the n sync signals." As discussed above, Simmonds does not disclose an array of external sync signals, but merely registers containing interrupt timing to prevent a race hazard. Neither Williams nor Simmonds discusses storing previous sync signals. Both Williams and Simmonds use the synchronization signals (Williams 0008, 0088, Simmonds col. 4, lines 14-20), but neither disclose storing the sync signals.

(4) Williams does not disclose "replacing the oldest of the n sync signals in the array with the n + 1 sync signal" as recited in claim 1. The Office Action asserts that "The clock signals of the graphics modules are the n sync signals since they are inherently the signals that were received previously, and the external synchronization signal is the n + 1 sync signal since it is the signal that is received next. ... The n sync signals are being replaced with the n + 1 sync signal, and therefore an oldest of the n sync signals is being replaced with the n + 1 sync signal."

The Office Action confuses two different parts of the invention in Williams. Williams discloses an external sync signal, which operates as the internal clock reference of the **slave graphics modules**, and the internal clock reference of the **master graphics module**. The Office Action confuses the internal clock reference of the slave graphics controller with the external sync signal. Aligning the internal clock reference with the sync signal is not the same as replacing the oldest of the n sync signals in the array with the n + 1 sync signal.

(A5) Srivastava does not disclose using the n + 1 sync signal to synchronize the at least one graphics processing card in each graphics processing computer with each at least one graphics processing card in the plurality of graphics processing computers if the comparisons of the n sync signals in the array are greater on the average than a preset threshold.

The Office Action suggests that Srivastava's threshold detector in combination with the error integrator which averages the output shows "synchronizing if the comparisons of the n sync signals are greater on average than a preset threshold." However, Srivastava's invention simply decides whether a correction of an oscillator may be a minor frequency correction or a large frequency correction. The minor frequency correction (Srivastava col. 6, lines 60-64) does not

require a long term change to prevent static phase error. The large frequency correction requires an appropriate long term change or shift of the steady state or free running frequency of the oscillator (Srivastava col. 8, lines 61-65). Srivastava thus assumes that the sync signal is valid and only uses a threshold to decide whether a long term frequency correction is an appropriate method. This assumption of validity and long term frequency correction decision is not the same as determining validity of the sync signal if the previous sync signal comparisons are greater than a threshold.

The Office Action relies on Williams, Simmonds and Srivastava to reject claims 1 and 10. The combination of Williams, Simmonds and Srivastava do not teach or suggest all of the elements of the invention as disclosed in independent claims 1 and 10. Therefore, Applicant respectfully submits that independent claims 1 and 10 are allowable, and urges the Examiner to withdraw the rejection.

Rejection of the dependent claims 2-5, 8-9, and 11-12 should be reconsidered and withdrawn for at least the reasons given above with respect to the independent claims. The dependent claims, being narrower in scope, are allowable for at least the reasons for which the independent claims are allowable.

CONCLUSION

In light of the above, Applicant respectfully submits that pending claims 1-13 are now in condition for allowance. Therefore, Applicant requests that the rejections and objections be withdrawn, and that the claims be allowed and passed to issue. If any impediment to the allowance of these claims remains after entry of this Amendment, the Examiner is strongly encouraged to call Steve Perry at (801) 566-6633 so that such matters may be resolved as expeditiously as possible.

Check No. 23349, in the amount of $60.00, is enclosed pursuant to 37 C.F.R. § 1.17(a)(1), for a one month extension of time pursuant to 37 C.F.R. § 1.136. No claims were added. Therefore, no additional fee is due.

The Commissioner is hereby authorized to charge any additional fee or to credit any overpayment in connection with this Amendment to Deposit Account No. 20-0100.

DATED this 6th day of October, 2005.

Respectfully submitted,

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